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EXAMINER	
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ART UNIT	PAPER NUMBER
2661	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,177	HOSPODOR ET AL.	
	Examiner	Art Unit	
	Joshua Kading	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☒ Claim(s) *5,6,8,12,16,17,19,23,25-27,29,32,34,35,38,39,41 and 147* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/28/00* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claims 2, 5, 6, 8, 12, 14, 16, 17, 19, 23, 25, 26, 27, 32, 34, 35, 38, 39, and 41 are objected to because of the following informalities:

Claim 2, line 2 states, "data". It should read, --the transmitted data--.

Claim 5, line 1 states, "data is queued". It should read, --the transmitted data is queued--.

Claim 6, line 1 states, "data". It should read, --the transmitted data--.

Cla states, "the data". It should read, --the transmitted data--.

Claim tes, "to other switched nodes". It should read, --to a plurality of other switched

Claim 10, lin witched fabric storage node". It should read, --switched node--.

Claim 12, line 2 states, "data". It should read, --the transmitted data--.

Claim 14, line 3 states, "data". It should read, --the transmitted data--.

Claim 16, line 1 states, "data". It should read, --the transmitted data--.

Claim 17, lines 1 and 2 state, "data". It should read, --the transmitted data--.

Claim 19, line 2 states, "linking nodes". It should read, --linking to a plurality of nodes--.

Claim 23, line 2 states, "data". It should read, --the transmitted data--.

Claim 25, line 3 states, "data". It should read, --the transmitted data--.

Claim 26, line 1 states, "data". It should read, --the transmitted data--.

Claim 27, lines 1 and 2 state, "data". It should read, --the transmitted data--.

Claim 32, line 2 states, "data". It should read, --the transmitted data--.

Claim 34, line 6 states, "writing data to and reading data from". It should read, --writing the stored data to and reading the stored data from--.

Claim 34, line 7 states, "data". It should read, --the stored data--.

Claim 34, line 12 states, "data". It should read, --the transmitted data--.

Claim 35, line 2 states, "data". It should read, --the transmitted data--.

Claim 38, line 1 states, "data". It should read, --the transmitted data--.

Claim 39, line 1 states, "data". It should read, --the transmitted data--.

Claim 39, line 1 states, "the data". It should read, --the transmitted data--.

Claim 41, line 2 states, "to other switched nodes". It should read, --to a plurality of other switched nodes--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, 11-20, 22-30, and 32-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. (U.S. Patent 5,600,638) in view of Fichou et al. (U.S. Patent 5,790,522).

In regard to claim 1, Bertin discloses "a switched node for use in a computer network comprising:(a) switching circuitry comprising more than two bi-directional ports for simultaneously transmitting data in multiple dimensions through the computer network (figure 3, elements 300, 301, and 302 where element 300 acts as the switching circuitry with switch 302, and bi-directional ports 301, where there are clearly more than two);

(b) a disk for storing data and a head actuated over the disk for writing data to and reading data from the disk (figure 3, element 306 where it is known in the art that a database, such as in figure 3, stores large quantities of data on a disk, like a hard disk, and retrieves the data using some sort of mechanical reader or head actuated over the disk)..."

However, Bertin lacks "...(c) a reservation facility for reserving resources associated with data read from the disk and written to the disk to support a predetermined Quality-of-Service constraint with respect to data transmitted through the computer network." Fichou however, discloses "...(c) a reservation facility for reserving resources associated with data read from the disk and written to the disk to support a predetermined Quality-of-Service constraint with respect to data transmitted through the computer network (figure 4, element 43 where the manager module 43 acts as the reservation facility to support the predetermined QoS as can be read in col. 6, lines 22-35 where the priority is a QoS constraint; it should also be noted that the input ports and output ports of figure 4 combined act as the bi-directional ports of Bertin)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the reservation facility with the rest of the switched node for the purpose of allowing higher priority data through before lower priority data. The motivation being that higher priority data can be switched and transmitted efficiently and on time.

In regard to claim 2, Bertin and Fichou disclose the node of claim 1. However, Bertin lacks "the resources comprise memory for buffering [the transmitted] data." Fichou however, further discloses "the resources comprise memory for buffering [the transmitted] data (figure 4, element 42)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the buffer with the node of claim 1 for the same reasons and motivation as in claim 1.

In regard to claim 3, Bertin and Fichou disclose the node of claim 1. However, Fichou lacks "the switching circuitry comprises a plurality of virtual lanes and the resources comprise at least one of the virtual lanes." Bertin however, further discloses "the switching circuitry comprises a plurality of virtual lanes and the resources comprise at least one of the virtual lanes (col. 10, lines 9-11 where the optimum routes act as the virtual lane chosen for the resources and by choosing implies that there are a plurality of virtual lanes for use by the switch; it should also be noted that although Bertin does not explicitly disclose virtual lanes, i.e. virtual circuits or paths, it is known in the art that with packet based communication systems there are virtual lanes that exist for each packet,

as they are the path from the source to the destination and do not necessarily include every route taken in between)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the virtual lanes with the node of claim 1 for the same reasons and motivation as in claim 1.

In regard to claim 4, Bertin and Fichou disclose the node of claim 3. However, Bertin lacks "each virtual lane comprises a predetermined priority level." Fichou however, further discloses "each virtual lane comprises a predetermined priority level (col. 2, line 64 where the connection refers to the virtual lane)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the priority level with the node of claim 3 for the same reasons and motivation as in claim 3.

In regard to claim 5, Bertin and Fichou disclose the node of claim 3. However, Bertin lacks "[the transmitted] data is queued within each virtual lane in order of arrival into the switched node." Fichou however, further discloses "[the transmitted] data is queued within each virtual lane in order of arrival into the switched node (figure 4, elements 42 where the "RT", "NRT", and "NR" queues represent different virtual lanes)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the queues with the node of claim 3 for the same reasons and motivation as in claim 3.

In regard to claim 6, Bertin and Fichou disclose the node of claim 3. However, Bertin lacks "[the transmitted] data is queued within each virtual lane with respect to transmission deadlines associated with the [transmitted] data." Fichou however, further discloses "[the transmitted] data is queued within each virtual lane with respect to transmission deadlines associated with the [transmitted] data (col. 3, lines 53-61 where the different queues again represent different delay-sensitive data or transmission deadlines for corresponding data)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the transmission deadlines with the node of claim 3 for the same reasons and motivation as in claim 3.

In regard to claim 7, Bertin and Fichou disclose the node of claim 1. However, Bertin lacks "the switching circuitry comprises processing circuitry and the resources comprise at least part of the processing circuitry." Fichou however, further discloses "the switching circuitry comprises processing circuitry and the resources comprise at least part of the processing circuitry (figure 4, element 43 where the switch and ports represent the switching circuitry of Bertin as defined in claim 1 and the manager module must have processing circuitry in it in order to function)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the processing circuitry with the node of claim 1 for the same reasons and motivation as in claim 1.

In regard to claim 8, Bertin and Fichou disclose the node of claim 1. However, Fichou lacks "(a) the switching circuitry comprises linking circuitry for linking to [a

plurality of] other switched nodes in the computer network; (b) the linking circuitry comprises a limited bandwidth; and (c) the resources comprise at least part of the linking circuitry bandwidth." Bertin however, further discloses "(a) the switching circuitry comprises linking circuitry for linking to [a plurality of] other switched nodes in the computer network (figure 3, elements 301 and 304 link the node to other nodes in the network); (b) the linking circuitry comprises a limited bandwidth (it is inherent in the design of all ports to have a limited bandwidth); and (c) the resources comprise at least part of the linking circuitry bandwidth (figure 3, element 301 where the ports contain the resources as in Fichou and the linking circuitry)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the linking circuitry with the node of claim 1 for the same reasons and motivation as in claim 1.

In regard to claim 9, Bertin and Fichou disclose the node of claim 1. However, Bertin lacks "(a) the switching circuitry comprises adapter circuitry for connecting to an external entity; and (b) the resources comprise at least part of the adapter circuitry." Fichou however, further discloses "(a) the switching circuitry comprises adapter circuitry for connecting to an external entity (figure 4, the XMT adapters connect the switching circuitry to an external entity); and (b) the resources comprise at least part of the adapter circuitry (figure 4, the XMT adapters queues contain the resources)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the adapters with the node of claim 1 for the same reasons and motivation as in claim 1.

In regard to claim 11, Bertin discloses "...disk drive comprising a head and a disk comprising a head and a disk (where it is known in the art that a database, such as in figure 3, stores large quantities of data on a disk, like a hard disk, and retrieves the data using some sort of mechanical reader or head actuated over the disk)..."

However, Bertin lacks "a method of reserving resources in a computer network to support a predetermined Quality-of-Service constraint with respect to a new access request to transmit data between a disk drive and a client computer, the computer network comprising a plurality of interconnected computer devices including a plurality of disk drives, each disk drive comprising a head and a disk, the method comprising the steps of: (a) finding at least one disk drive out of the plurality of disk drives that can service the new access request while supporting the Quality-of-Service constraint for the new and existing access requests; and (b) reserving resources within the at least one disk drive to service the new access request."

Fichou however, discloses "a method of reserving resources in a computer network to support a predetermined Quality-of-Service constraint with respect to a new access request to transmit data between a disk drive and a client computer, the computer network comprising a plurality of interconnected computer devices including a plurality of disk drives, each disk drive comprising a head and a disk, the method comprising the steps of: (a) finding at least one disk drive out of the plurality of disk drives that can service the new access request while supporting the Quality-of-Service constraint for the new and existing access requests (col. 2, lines 35-41 where the network contains a plurality of nodes each containing a hard disk as in figure 1); and (b)

reserving resources within the at least one disk drive to service the new access request (col. 2, lines 26-34)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the disk drive with the rest of the method for the purpose of having a data storage unit. The motivation being that each switching unit is computerized and needs a data storage unit to manage and change network topology information effectively.

In regard to claim 12, Bertin and Fichou disclose the method of claim 11. However, Bertin lacks "the resources comprise memory for buffering [the transmitted] data." Fichou however, further discloses "the resources comprise memory for buffering [the transmitted] data (figure 4, element 42)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the buffer with the method of claim 11 for the same reasons and motivation as in claim 11.

In regard to claim 13, Bertin and Fichou disclose the method of claim 11. However, Fichou lacks "the resources comprise network circuitry for communicating with the computer network." Bertin however, further discloses "the resources comprise network circuitry for communicating with the computer network (figure 3, elements 301 and 304 are used to communicate with the computer network as in figure 2)." It would have been obvious to one with ordinary skill in the art at the time of invention to include

the network circuitry with the method of claim 11 for the same reasons and motivation as in claim 11.

In regard to claim 14, Bertin and Fichou disclose the method of claim 13. However, Fichou lacks "(a) the network circuitry comprises multi-port switching circuitry for simultaneously transmitting [the transmitted] data in multiple dimensions through the computer network; and (b) the resources comprise a virtual lane within the multi-port switching circuitry." Bertin however, further discloses "(a) the network circuitry comprises multi-port switching circuitry for simultaneously transmitting [the transmitted] data in multiple dimensions through the computer network (figure 3, elements 301 and 304 show the multi-port circuitry and there are clearly multiple dimensions to transmit as each 301 has a different dimension); and (b) the resources comprise a virtual lane within the multi-port switching circuitry (col. 10, lines 9-11 where the optimum routes act as the virtual lane chosen for the resources; it should also be noted that although Bertin does not explicitly disclose virtual lanes, i.e. virtual circuits or paths, it is known in the art that with packet based communication systems there are virtual lanes that exist for each packet, as they are the path from the source to the destination and do not necessarily include every route taken in between)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the multi-port circuitry with the method of claim 13 for the same reasons and motivation as in claim 13.

In regard to claim 15, Bertin and Fichou disclose the method of claim 14. However, Bertin lacks "each virtual lane comprises a predetermined priority level." Fichou however, further discloses "each virtual lane comprises a predetermined priority level (col. 2, line 64 where the connection refers to the virtual lane)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the priority level with the method of claim 14 for the same reasons and motivation as in claim 14.

In regard to claim 16, Bertin and Fichou disclose the node of claim 14. However, Bertin lacks "[the transmitted] data is queued within each virtual lane in order of arrival into the switched node." Fichou however, further discloses "[the transmitted] data is queued within each virtual lane in order of arrival into the switched node (figure 4, elements 42 where the "RT", "NRT", and "NR" queues represent different virtual lanes)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the queues with the method of claim 14 for the same reasons and motivation as in claim 14.

In regard to claim 17, Bertin and Fichou disclose the method of claim 14. However, Bertin lacks "[the transmitted] data is queued within each virtual lane with respect to transmission deadlines associated with the [transmitted] data." Fichou however, further discloses "[the transmitted] data is queued within each virtual lane with respect to transmission deadlines associated with the [transmitted] data (col. 3, lines 53-61 where the different queues again represent different delay-sensitive data or

transmission deadlines for corresponding data)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the transmission deadlines with the method of claim 14 for the same reasons and motivation as in claim 14.

In regard to claim 18, Bertin and Fichou disclose the method of claim 14. However, Bertin lacks "the multi-port switching circuitry comprises processing circuitry and the resources comprise at least part of the processing circuitry." Fichou however, further discloses "the multi-port switching circuitry comprises processing circuitry and the resources comprise at least part of the processing circuitry (figure 4, element 43 where the switch and ports represent the switching circuitry of Bertin and the manager module must have processing circuitry in it in order to function)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the processing circuitry with the method of claim 14 for the same reasons and motivation as in claim 14.

In regard to claim 19, Bertin and Fichou disclose the method of claim 14. However, Fichou lacks "(a) the multi-port switching circuitry comprises linking circuitry for linking [a plurality of] nodes in the computer network; (b) the linking circuitry comprises a limited bandwidth; and (c) the resources comprise at least part of the linking circuitry bandwidth." Bertin however, further discloses "(a) the multi-port switching circuitry comprises linking circuitry for linking [a plurality of] nodes in the computer network (figure 3, elements 301 and 304 link the node to other nodes in the

network); (b) the linking circuitry comprises a limited bandwidth (it is inherent in the design of all ports to have a limited bandwidth); and (c) the resources comprise at least part of the linking circuitry bandwidth (figure 3, element 301 where the ports contain the resources as in Fichou and the linking circuitry)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the linking circuitry with the method of claim 14 for the same reasons and motivation as in claim 14.

In regard to claim 20, Bertin and Fichou disclose the method of claim 14. However, Bertin lacks "(a) the multi-port switching circuitry comprises adapter circuitry for connecting to an external entity; and (b) the resources comprise at least part of the adapter circuitry." Fichou however, further discloses "(a) the multi-port switching circuitry comprises adapter circuitry for connecting to an external entity (figure 4, the XMIT adapters connect the switching circuitry to an external entity); and (b) the resources comprise at least part of the adapter circuitry (figure 4, the XMIT adapters queues contain the resources)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the adapters with the method of claim 14 for the same reasons and motivation as in claim 14.

In regard to claim 22, Bertin discloses "a computer network comprising: (a) a plurality of interconnected computer devices including a plurality of client computers and a plurality of disk drives for storing network data, each disk drive comprising a head and a disk (figure 2, where it is clear there a plurality of client computers and disk drives;

figure 3, element 306 represents a disk drive with a head and disk as is known in the art; it should also be noted that figure 3 is a node of figure 2 as can be read in col. 8, lines 14-18); (b) a plurality of interconnected nodes (figure 2, where the nodes are clearly connected)..."

However, Bertin lacks "...(c) a reservation facility for reserving resources within the disk drives and the nodes to support a predetermined Quality-of-Service constraint with respect to data transmitted between the disk drives and the client computers through the nodes of the computer network."

Fichou however, discloses "...(c) a reservation facility for reserving resources within the disk drives and the nodes to support a predetermined Quality-of-Service constraint with respect to data transmitted between the disk drives and the client computers through the nodes of the computer network (figure 4, element 43 where the manager module 43 acts as the reservation facility to support the predetermined QoS as can be read in col. 6, lines 22-35 where the priority is a QoS constraint; it should also be noted that the input ports and output ports of figure 4 combined act as the bi-directional ports of Bertin)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the reservation facility with the rest of the network for the purpose of allowing higher priority data through before lower priority data. The motivation being that higher priority data can be switched and transmitted efficiently and on time.

In regard to claim 23, Bertin and Fichou disclose the network of claim 22. However, Bertin lacks "the resources comprise memory for buffering [the transmitted] data." Fichou however, further discloses "the resources comprise memory for buffering [the transmitted] data (figure 4, element 42)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the buffer with the network of claim 22 for the same reasons and motivation as in claim 22.

In regard to claim 24, Bertin and Fichou disclose the network of claim 22. However, Fichou lacks "the resources comprise network circuitry for communicating with the computer network." Bertin however, further discloses "the resources comprise network circuitry for communicating with the computer network (figure 3, elements 301 and 304 are used to communicate with the computer network as in figure 2)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the network circuitry with the network of claim 22 for the same reasons and motivation as in claim 22.

In regard to claim 25, Bertin and Fichou disclose the network of claim 24. However, Fichou lacks "(a) the network circuitry comprises multi-port switching circuitry for simultaneously transmitting [the transmitted] data in multiple dimensions through the computer network; and (b) the resources comprise a virtual lane within the multi-port switching circuitry." Bertin however, further discloses "(a) the network circuitry comprises multi-port switching circuitry for simultaneously transmitting [the transmitted]

data in multiple dimensions through the computer network (figure 3, elements 301 and 304 show the multi-port circuitry and there are clearly multiple dimensions to transmit as each 301 has a different dimension); and (b) the resources comprise a virtual lane within the multi-port switching circuitry (col. 10, lines 9-11 where the optimum routes act as the virtual lane chosen for the resources; it should also be noted that although Bertin does not explicitly disclose virtual lanes, i.e. virtual circuits or paths, it is known in the art that with packet based communication systems there are virtual lanes that exist for each packet, as they are the path from the source to the destination and do not necessarily include every route taken in between)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the multi-port circuitry with the network of claim 24 for the same reasons and motivation as in claim 24.

In regard to claim 26, Bertin and Fichou disclose the network of claim 25. However, Bertin lacks "[the transmitted] data is queued within each virtual lane in order of arrival into the switched node." Fichou however, further discloses "[the transmitted] data is queued within each virtual lane in order of arrival into the switched node (figure 4, elements 42 where the "RT", "NRT", and "NR" queues represent different virtual lanes)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the queues with the network of claim 25 for the same reasons and motivation as in claim 25.

In regard to claim 27, Bertin and Fichou disclose the network of claim 25. However, Bertin lacks "[the transmitted] data is queued within each virtual lane with respect to transmission deadlines associated with the [transmitted] data." Fichou however, further discloses "[the transmitted] data is queued within each virtual lane with respect to transmission deadlines associated with the [transmitted] data (col. 3, lines 53-61 where the different queues again represent different delay-sensitive data or transmission deadlines for corresponding data)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the transmission deadlines with the network of claim 25 for the same reasons and motivation as in claim 25.

In regard to claim 28, Bertin and Fichou disclose the network of claim 25. However, Bertin lacks "the multi-port switching circuitry comprises processing circuitry and the resources comprise at least part of the processing circuitry." Fichou however, further discloses "the multi-port switching circuitry comprises processing circuitry and the resources comprise at least part of the processing circuitry (figure 4, element 43 where the switch and ports represent the switching circuitry of Bertin and the manager module must have processing circuitry in it in order to function)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the processing circuitry with the network of claim 25 for the same reasons and motivation as in claim 25.

In regard to claim 29, Bertin and Fichou disclose the network of claim 25. However, Fichou lacks "(a) the multi-port switching circuitry comprises linking circuitry for linking the nodes in the computer network; (b) the linking circuitry comprises a limited bandwidth; and (c) the resources comprise at least part of the linking circuitry bandwidth." Bertin however, further discloses "(a) the multi-port switching circuitry comprises linking circuitry for linking the nodes in the computer network (figure 3, elements 301 and 304 link the node to other nodes in the network); (b) the linking circuitry comprises a limited bandwidth (it is inherent in the design of all ports to have a limited bandwidth); and (c) the resources comprise at least part of the linking circuitry bandwidth (figure 3, element 301 where the ports contain the resources as in Fichou and the linking circuitry)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the linking circuitry with the network of claim 25 for the same reasons and motivation as in claim 25.

In regard to claim 30, Bertin and Fichou disclose the network of claim 25. However, Bertin lacks "(a) the multi-port switching circuitry comprises adapter circuitry for connecting to an external entity; and (b) the resources comprise at least part of the adapter circuitry." Fichou however, further discloses "(a) the multi-port switching circuitry comprises adapter circuitry for connecting to an external entity (figure 4, the XMIT adapters connect the switching circuitry to an external entity); and (b) the resources comprise at least part of the adapter circuitry (figure 4, the XMIT adapters queues contain the resources)." It would have been obvious to one with ordinary skill in the art

at the time of invention to include the adapters with the network of claim 25 for the same reasons and motivation as in claim 25.

In regard to claim 32, Bertin and Fichou disclose the network of claim 22. However, Fichou lacks "each node comprises multi-port switching circuitry for simultaneously transmitting [the transmitted] data in multiple dimensions through the computer network." Bertin however, further discloses "the network circuitry comprises multi-port switching circuitry for simultaneously transmitting [the transmitted] data in multiple dimensions through the computer network (figure 3, elements 301 and 304 show the multi-port circuitry and there are clearly multiple dimensions to transmit as each 301 has a different dimension)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the switching circuitry with the network of claim 22 for the same reasons and motivation as in claim 22.

In regard to claim 33, Bertin discloses "a computer network comprising: (a) a plurality of interconnected computer devices including a plurality of client computers and a plurality of disk drives for storing network data, the disk drives each comprising a head and a disk (figure 2, where it is clear there a plurality of client computers and disk drives; figure 3, element 306 represents a disk drive with a head and disk as is known in the art; it should also be noted that figure 3 is a node of figure 2 as can be read in col. 8, lines 14-18); (b) a plurality of interconnected nodes (figure 2, where the nodes are clearly connected)..."

However, Bertin lacks "...(c) a reservation facility for reserving resources within the disk drives and the nodes to support a predetermined Quality-of-Service constraint with respect to data transmitted between the disk drives through the nodes of the computer network."

Fichou however, discloses "...(c) a reservation facility for reserving resources within the disk drives and the nodes to support a predetermined Quality-of-Service constraint with respect to data transmitted between the disk drives through the nodes of the computer network (figure 4, element 43 where the manager module 43 acts as the reservation facility to support the predetermined QoS as can be read in col. 6, lines 22-35 where the priority is a QoS constraint; it should also be noted that the input ports and output ports of figure 4 combined act as the bi-directional ports of Bertin)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the reservation facility with the rest of the network for the purpose of allowing higher priority data through before lower priority data. The motivation being that higher priority data can be switched and transmitted efficiently and on time.

In regard to claim 34, Bertin discloses "a switched fabric computer network comprising: (a) a plurality of interconnected nodes for simultaneously transmitting data in multiple dimensions through the computer network (figure 2 shows the interconnected nodes and figure 3, elements 301 and 304 show circuitry for transmitting through multiple dimensions), each node comprising: switching circuitry comprising more than two bi-directional ports (figure 3, elements 300, 301, and 302 where element 300 acts

as the switching circuitry with switch 302, and bi-directional ports 301, where there are clearly more than two); a disk for storing data (figure 3, element 306); and a head actuated over the disk for writing [the stored] data to and reading [the stored] data from the disk (figure 3, element 306 where it is known in the art that databases are storage devices that contain large amounts of data on a disk and, as is known in the art, the disk is read and written to with an actuated head)..."

However, Bertin lacks "...(b) a reservation facility for reserving resources associated with [the stored] data read from the disk and written to the disk to support a predetermined Quality-of-Service constraint with respect to data transmitted between the interconnected nodes and client computers connected to the switched fabric computer network; and (c) a scheduling facility, responsive to the resources reserved by the reservation facility, for scheduling the transmission of [the transmitted] data through the interconnected nodes to support the predetermined Quality-of-Service constraint."

Fichou however, discloses "...(b) a reservation facility for reserving resources associated with [the stored] data read from the disk and written to the disk to support a predetermined Quality-of-Service constraint with respect to data transmitted between the interconnected nodes and client computers connected to the switched fabric computer network (figure 4, element 43 where the manager module 43 acts as the reservation facility to support the predetermined QoS as can be read in col. 6, lines 22-35 where the priority is a QoS constraint; it should also be noted that the input ports and output ports of figure 4 combined act as the bi-directional ports of Bertin); and (c) a scheduling facility, responsive to the resources reserved by the reservation facility, for

scheduling the transmission of [the transmitted] data through the interconnected nodes to support the predetermined Quality-of-Service constraint (figure 4, in the XMIT adapters there is a scheduler or scheduling facility)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the reservation facility and the scheduling facility with the rest of the network for the purpose of allowing higher priority data through before lower priority data. The motivation being that higher priority data can be switched and transmitted efficiently and on time.

In regard to claim 35, Bertin and Fichou disclose the network of claim 34. However, Bertin lacks "the resources comprise memory for buffering [the transmitted] data." Fichou however, further discloses "the resources comprise memory for buffering [the transmitted] data (figure 4, element 42)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the buffer with the network of claim 34 for the same reasons and motivation as in claim 34.

In regard to claim 36, Bertin and Fichou disclose the network of claim 34. However, Fichou lacks "the resources comprise network circuitry for communicating with the switched fabric computer network." Bertin however, further discloses "the resources comprise network circuitry for communicating with the switched fabric computer network (figure 3, elements 301 and 304 are used to communicate with the computer network as in figure 2)." It would have been obvious to one with ordinary skill

in the art at the time of invention to include the network circuitry with the network of claim 34 for the same reasons and motivation as in claim 34.

In regard to claim 37, Bertin and Fichou disclose the network of claim 34. However, Fichou lacks "the switching circuitry comprises a plurality of virtual lanes and the resources comprise at least one of the virtual lanes." Bertin however, further discloses "the switching circuitry comprises a plurality of virtual lanes and the resources comprise at least one of the virtual lanes (col. 10, lines 9-11 where the optimum routes act as the virtual lane chosen for the resources and by choosing implies that there are a plurality of virtual lanes for use by the switch; it should also be noted that although Bertin does not explicitly disclose virtual lanes, i.e. virtual circuits or paths, it is known in the art that with packet based communication systems there are virtual lanes that exist for each packet, as they are the path from the source to the destination and do not necessarily include every route taken in between)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the virtual lanes with the network of claim 34 for the same reasons and motivation as in claim 34.

In regard to claim 38, Bertin and Fichou disclose the network of claim 37. However, Bertin lacks "[the transmitted] data is queued within each virtual lane in order of arrival into the switched node." Fichou however, further discloses "[the transmitted] data is queued within each virtual lane in order of arrival into the switched node (figure 4, elements 42 where the "RT", "NRT", and "NR" queues represent different virtual

lanes)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the queues with the network of claim 37 for the same reasons and motivation as in claim 37.

In regard to claim 39, Bertin and Fichou disclose the network of claim 37. However, Bertin lacks "[the transmitted] data is queued within each virtual lane with respect to transmission deadlines associated with the [transmitted] data." Fichou however, further discloses "[the transmitted] data is queued within each virtual lane with respect to transmission deadlines associated with the [transmitted] data (col. 3, lines 53-61 where the different queues again represent different delay-sensitive data or transmission deadlines for corresponding data)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the transmission deadlines with the network of claim 37 for the same reasons and motivation as in claim 37.

In regard to claim 40, Bertin and Fichou disclose the network of claim 34. However, Bertin lacks "the switching circuitry comprises processing circuitry and the resources comprise at least part of the processing circuitry." Fichou however, further discloses "the switching circuitry comprises processing circuitry and the resources comprise at least part of the processing circuitry (figure 4, element 43 where the switch and ports represent the switching circuitry of Bertin as defined in claim 1 and the manager module must have processing circuitry in it in order to function)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the

processing circuitry with the network of claim 34 for the same reasons and motivation as in claim 34.

In regard to claim 41, Bertin and Fichou disclose the network of claim 34. However, Fichou lacks "(a) the switching circuitry comprises linking circuitry for linking to [a plurality of] other switched nodes in the computer network; (b) the linking circuitry comprises a limited bandwidth; and (c) the resources comprise at least part of the linking circuitry bandwidth." Bertin however, further discloses "(a) the switching circuitry comprises linking circuitry for linking to [a plurality of] other switched nodes in the computer network (figure 3, elements 301 and 304 link the node to other nodes in the network); (b) the linking circuitry comprises a limited bandwidth (it is inherent in the design of all ports to have a limited bandwidth); and (c) the resources comprise at least part of the linking circuitry bandwidth (figure 3, element 301 where the ports contain the resources as in Fichou and the linking circuitry)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the linking circuitry with the network of claim 34 for the same reasons and motivation as in claim 34.

In regard to claim 42, Bertin and Fichou disclose the network of claim 34. However, Bertin lacks "(a) the switching circuitry comprises adapter circuitry for connecting to an external entity; and (b) the resources comprise at least part of the adapter circuitry." Fichou however, further discloses "(a) the switching circuitry comprises adapter circuitry for connecting to an external entity (figure 4, the XMT

adapters connect the switching circuitry to an external entity); and (b) the resources comprise at least part of the adapter circuitry (figure 4, the XMT adapters queues contain the resources)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the adapters with the network of claim 34 for the same reasons and motivation as in claim 34.

Claims 10, 21, 31, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. and Fichou et al. as applied to claims 1, 11, 22, and 34 respectively, and further in view of Stolfo (U.S. Patent 5,668,897).

In regard to claim 10, Bertin and Fichou disclose the node of claim 1. However, Bertin and Fichou lack "the reservation facility limits movement of the head so as to constrain the head to a predetermined region of the disk, thereby reserving a resource within the switched fabric storage node." Stolfo however, discloses "the reservation facility limits movement of the head so as to constrain the head to a predetermined region of the disk, thereby reserving a resource within the switched fabric storage node (col. 22, lines 51-56 where the head is constrained to a given region; it should also be noted that although Stolfo discusses a CD-ROM, the same principle applies to all disk with head type storage devices)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the constrained movement with the node of claim 1 for the purpose of minimizing the movement of the head as much as possible.

The motivation being that the less the head has to move to access a region, the quicker the data from that region can be retrieved or written.

In regard to claim 21, Bertin and Fichou disclose the method of claim 11. However, Bertin and Fichou lack "the step of reserving resources comprises the step of limiting movement of the head so as to constrain the head to a predetermined region of the disk." Stolfo however, discloses "the step of reserving resources comprises the step of limiting movement of the head so as to constrain the head to a predetermined region of the disk (col. 22, lines 51-56 where the head is constrained to a given region; it should also be noted that although Stolfo discusses a CD-ROM, the same principle applies to all disk with head type storage devices)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the constrained movement with the method of claim 11 for the purpose of minimizing the movement of the head as much as possible. The motivation being that the less the head has to move to access a region, the quicker the data from that region can be retrieved or written.

In regard to claim 31, Bertin and Fichou disclose the network of claim 22. However, Bertin and Fichou lack "the reservation facility limits movement of the head so as to constrain the head to a predetermined region of the disk, thereby reserving a resource within the switched fabric storage node." Stolfo however, discloses "the reservation facility limits movement of the head so as to constrain the head to a predetermined region of the disk, thereby reserving a resource within the switched

fabric storage node (col. 22, lines 51-56 where the head is constrained to a given region; it should also be noted that although Stolfo discusses a CD-ROM, the same principle applies to all disk with head type storage devices)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the constrained movement with the network of claim 22 for the purpose of minimizing the movement of the head as much as possible. The motivation being that the less the head has to move to access a region, the quicker the data from that region can be retrieved or written.

In regard to claim 43, Bertin and Fichou disclose the network of claim 34. However, Bertin and Fichou lack "the reservation facility limits movement of the head so as to constrain the head to a predetermined region of the disk, thereby reserving a resource within the switched fabric storage node." Stolfo however, discloses "the reservation facility limits movement of the head so as to constrain the head to a predetermined region of the disk, thereby reserving a resource within the switched fabric storage node (col. 22, lines 51-56 where the head is constrained to a given region; it should also be noted that although Stolfo discusses a CD-ROM, the same principle applies to all disk with head type storage devices)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the constrained movement with the network of claim 34 for the purpose of minimizing the movement of the head as much as possible. The motivation being that the less the head has to move to access a region, the quicker the data from that region can be retrieved or written.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Kading whose telephone number is (703) 305-0342. The examiner can normally be reached on M-F: 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Olms can be reached on (703) 305-4703. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Joshua Kading
Examiner
Art Unit 2661

JK
December 30, 2003

KENNETH VANDERPUYE
PRIMARY EXAMINER